Digital rf controller logic architecture and configuration

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The National Synchrotron Light Source II accelerator consists of the storage ring, booster ring, and injector subsystem [], the last containing linacs, buncher, prebuncher, and sub-harmonic buncher cavities. The rf components of the storage ring consists of four CESR-type superconducting (SC) cavities [] and two higher-harmonic cavities for lengthening bunches. NSLS is committed to the use of digital rf controllers for controlling them []. These controllers have eight analog-to-digital converter (ADC) channels converting signals running at the first intermediate frequency (IF) to the second IF frequency using I/Q detection [] resulting in a real data stream containing interleaved I and Q components.

INTRODUCTION

The National Synchrotron Light Source II accelerator [1] consists of the storage ring, booster ring, and injector subsystem, the last containing linacs, buncher, and sub-harmonic buncher cavities. The rf components of the storage ring consists of four CESR-type superconducting (SC) cavities and two higher-harmonic cavities [2] for lengthening bunches. NSLS is committed to the use of digital rf controllers for controlling them [3]. These controllers have eight analog-to-digital converter (ADC) channels converting signals running at the first intermediate frequency (IF) to the second IF frequency using I/Q detection resulting in a real data stream containing interleaved I and Q components.

Given the number, types, and variety of functions of these cavities, we naturally sought to limit logic development effort by reuse of code. We did this by the use of generic parameterized modules below the top level of the logic design wherever possible, e.g., constructing state machines from timer and linear-state-sequencer building blocks, registers, and accumulators in structural descriptions of the logic above the lowest levels of the design.

At the top level of the design, we used conditional compilation (Verilog `defines) to instantiate functions as needed. For example, instantiation of feedback, interlock components such as quench detection, and ramp generators are conditional depending on the needs of the rf system towards which the build is targeted. This way, even the top-level logic is common to all systems, including unpowered systems, and only one design needs to be tracked. Data paths bypassing uninstantiated blocks are seamlessly tied to the next instantiated block, and instantiated blocks have controls and diagnostics automatically tied to their host-interface sources and destinations. Local nodes are declared where they are used and are not instantiated when their blocks are not.

ADC and digital-to-analog converter (DAC) bit widths are parameterized, and all data-path widths internal to the design are tied to, or influenced by, these parameters – making the design agile with respect to the choice of ADC and DAC chips.

During the time between introduction of a new rf board version and retirement of the old, Verilog symbols are also used to distinguish versions, and select appropriate input and output pin assignments that are dependent on these targets. Separate Xilinx project files are used for different board targets because different pin files (Xilinx .ucf files) are linked to the build. Otherwise the projects are identical.

UNIVERSAL FUNCTIONS IN LOGIC

There are a handful of functions in logic that are universal across the targets of the build. These functions include ADC signal acquisition and demultiplexing, the scope and circular-buffer diagnostics, serial number, and host interface.

The four on-board ADC chips provide eight channels in four double-data-rate data streams, which are demultiplexed by a module parameterized for bit width. Four of the ADC channels containing the rf reference, cavity field, forward, and reverse signals are assigned standard names, the last two locally only in powered systems.

They and four other signals are available to an eight-channel scope function that has assigned to it a block-transfer mechanism to the host. This is useful diagnostic function, providing waveforms to the host, and flexible triggering configured at build time.

The circular buffer is built around a 32-Mbyte sdram chip. It is configured to continuously acquire five chan-

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nels, wrapping to the beginning. When triggered by trips or other source, it continues to acquire half its capacity, after which acquisition is stopped and its data downloaded.

The host interface currently is the logic portion of the Opal Kelly product FrontPanel. An Ethernet interface in logic [] will later be available and selectable via a build option. The physical interface is already in place.

A Maxim DS1825 chip in the rf board provides a unique serial number for the board. Logic build options are also available to the host through the host interface. With these two codes, both the board and its logic configuration are always known to the host.

POWERED SYSTEMS, CAVITY TUNING

Powered systems are those systems whose cavity is powered by an rf amplifier (the only unpowered system type is for the Landau cavities.) These systems are configured with logic to generate an IF2 signal that is upconverted and routed the amplifier chain. The source of this IF2 signal is a waveform table whose I/Q waypoints can be clocked out at varying rates. This waveform table, termed the feed-forward setpoint table (ff table) is useful not just for simply powering the cavity, but for response measurements in both the frequency domain, as mentioned earlier, and time domain via pulse waveforms.

Feedback

Systems with feedback are configured with set-point generation and feedback gains. The amplified error is then combined with the system's ff-table output prior to up conversion.

Fixed field set points (I and Q parts) controlled by the host are provided for all target systems with feedback except for the booster. Because the booster is ramped through its cycle, a ramp table in logic that linearly interpolates between 512 I/Q waypoints is compiled into its build. This table, like the feed-forward table, are loaded by block transfers from the host interface. When the build target is instead a CESR cavity system for the storage ring, a distinct ramp block that ramps the fixed field set point to zero over about a millisecond is instantiated in the set-point chain. This block provides a more gentle rf shutoff in response to non-critical trips [clsrampdown].

Feedback gains are implemented in a parameterized module having proportional and integral paths. Proportional gain and feedback-loop phase adjustments are via a complex multiplier to which a constant I/Q multiplier is applied. Integral gain adjustment is chained to proportional gain so that integral gain alone controls the feedback's time constant. Coarse gains of the proportional and integral paths are independently setable by parameters controlling bit offsets of the feedback input relative to the output. Besides overall gain being adjustable using these parameters, their relative gains, which need to be adjustable as a means to accommodate wide variation of rf cavity time constants with the use of different cavity technologies, particularly normal-conducting (NC) vs. superconducting flag (SC), are also adjustable. Earlier incarnations used a simple NC/SC flag fixing these bit offsets.

Parameterized input and output bit widths to/from this module are tied to ADC+1 and DAC bit widths, respectively, and internal data paths have additional bits. Some of these bits are there to prevent overflow. Other least-significant bits (lsbs) are there to limit introduction of quantization error during sums of multiple terms, bits that are discarded only after summation. A parameterized saturation module permits reduction of the number of bits of a data path, while preserving gain, without overflow that would otherwise occur via wrapping in the fixed-width arithmetic.

Interlocks, limiter, and up conversion

A variety of external and internal interlock source signals, such as amplifier fault, quench, and software triggers, are routed to destinations via an interlock matrix whose rows are logic ored to provide the final trigger to the destination. This matrix, although in its current form is clumsy to configure, allows flexible configuration of interlocks. The configuration of the project provides that unconnected signals are pulled to ground by default, so that unconnected matrix elements are at logic zero. In this way, unconnected matrix elements due to no connection or uninstantiated logic do not need to be explicitly tied to logic zero. Besides having software resets, all interlock latches have a software trip to facilitate testing.

A constant-phase limiter is instantiated in the drive chain. It is constructed from a parameterized serial Cordic module that results in a response time of about 16 clock cycles. It can be disabled via host logic and its limiting level is coded as a parameter in logic.

First up conversion from the digital fs/4- (IF2) to 5 fs/4-IF (IF1) frequency at a double sample rate (2 fs) is performed prior to digital-to-analog conversion [doolittle]. A simple filter removes the unwanted lines. This function, too, is performed by a parameterized module whose bit width is tied to the DAC bit width when it is instantiated in logic.

Response measurements in powered systems

Time-domain response measurements are possible using the ff table loaded with a suitable pulse waveform. Time constants are readily extracted this way. With feedback, gains can be adjusted to the threshold of ringing. In a test at CLS, the proportional and integral gains could be independently adjusted this way because of the differing time scales of their ringing.

The ff table and circular buffer are also used as a frequency-domain network analyzer. To do this, the ff table is first loaded with one-or-more cycles of sine wave and set to output continuously at a given rate to effect excitation of the system at some frequency. The circular buffer acquires its full capacity of data after transients are allowed to damp, down loaded, clipped to an integral multiple of excitation cycles, and Fourier analyzed to determine a frequency response point. The ff-table output itself is also sampled and serves as a reference.

Cavity tuning

HOST INTERFACE

A unique rf-board specific serial number from a Dallas serial-number chip is available to the host through the host interface. Furthermore, all options specified for the build of the logic are accessible to the host. This way the host is always aware of the identity of the board and the configuration of loaded logic. A configuration parameter is available to control instantiation of the host interface. At this point only a commercial USB-based board is tied into the rf logic. It is anticipated that an ethernet interface will later be available and selectable in logic via a symbol.

SUMMARY

[1] F. Willeke, Conf.Proc. **C110328**, 732 (2011).

[2] J. Rose, S. Sharma, R. Sikora, W. Gash, B. Kosciuk, *et al.*, Conf.Proc. **C110328**, 910 (2011).

[3] J. Cupolo, R. Sikora, B. Holub, H. Ma, J. Oliva, *et al.*, Conf.Proc. **C110328**, 669 (2011).